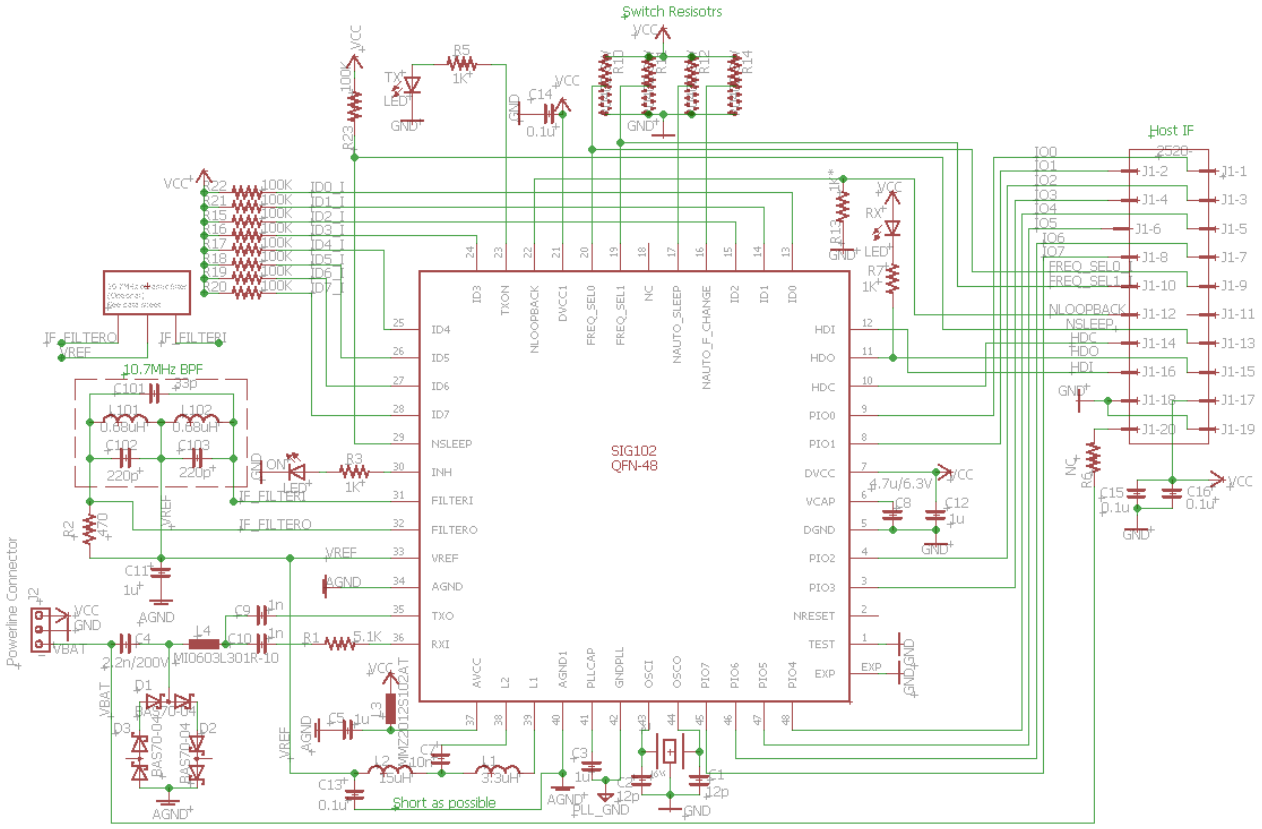
YAMAR	SIG102 Ref Board R1_4 Assembly	www.yamar.com

1. SIG102 Ref board schematic



See SIG102 data sheet http://www.yamar.com/datasheet/DS-SIG102.pdf

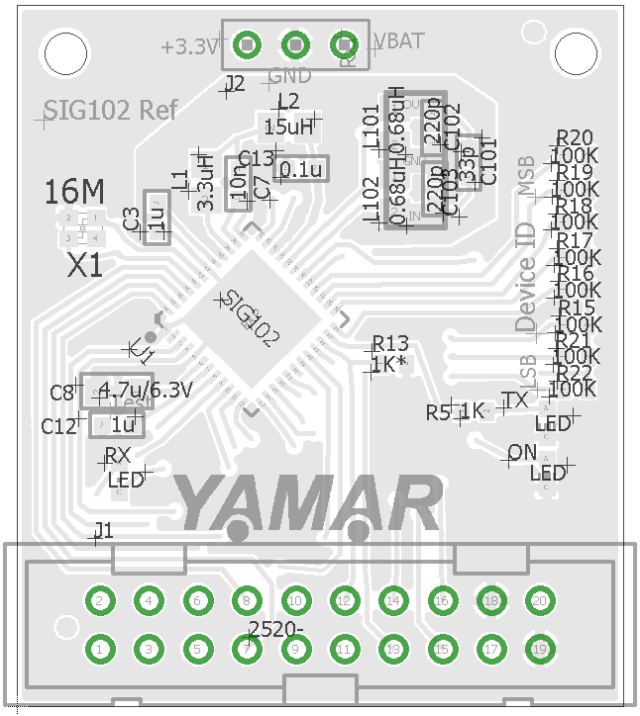
2. SIG102 BOM

Qty	Value	Device	Package	Parts	Description
4	0.1u	C0603	C0603	C13, C14, C15, C16	CAPACITOR
2	0.68uH	L0805	R0805	L101, L102	INDUCTOR
9	100K	RR0402	R0402	R15, R16, R17, R18, R19, R20, R21, R22, R23	RESISTOR
1	10n	C0603	C0603	C7	CAPACITOR
2	12p	C0603	C0603	C1, C2	CAPACITOR
1	15uH	L2	R0805	L2	Abracon 815-AIML-0805-150K-T
1	16M	XTAL_16M	IQG2016	X1	NDK NX2016SA-16MHz SMD, 2.0x1.6 mm
3	1K	RR0402	R0402	R3, R5, R7	RESISTOR
1	1K*	RR0402	R0402	R13	RESISTOR
2	1n	C0603	C0603	C9, C10	CAPACITOR
4	1u	C0603	C0603	C3, C5, C11, C12	CAPACITOR
1	2.2n/200V	C0805	C0805	C4	CAPACITOR
2	220p	C0603	C0603	C102, C103	CAPACITOR
1	2520-	2520-	PAK100/2500-20	J1	3M (TM) Pak 100 4-Wall Header
1	3.3uH	L1	R0805	L1	Abracon 815-AIML-0805-3R3K-T
1	33p	C0603	C0603	C101	CAPACITOR
1	4.7u/6.3V	C0805	C0805	C8	CAPACITOR
1	470	RR0402	R0402	R2	RESISTOR
1	5.1K	RR0402	R0402	R1	RESISTOR
3	BAS70-04	BAS70-04	SOT23	D1, D2, D3	BAS70-04 Silicon Schottky Diodes
1	FILTER-SMD	FILTERSMF	SMF	F-SMD	Optional 10.7MHz ceramic filter, replacing the discrete filter
2	LED	LEDCHIP-LED0603	CHIP-LED0603	ON, TX	LED
1	LED	LEDCHIPLED_0603	CHIPLED_0603	RX	LED
1	MI0603L301R-10	MI0603L301R-10	R0805	L4	Optional for EMC usage LAIRD - MI0603L301R-10, else place 0 Ohm resistor
1	MMZ2012S102AT	MMZ2012S102AT	R0805	L3	TDK MMZ2012S102AT
1	NC	RR0402	R0402	R6	RESISTOR
1	Powerline Connector	MTA03-100	10X03MTA	J2	AMP connector
4	R0402-SW	R0402-SW	SW-R0402	R10, R11, R12, R14	SWITCH RESISTOR
1	SIG102	SIG102	QFN48	U1	Yamar SIG102 powerline transceiver IC

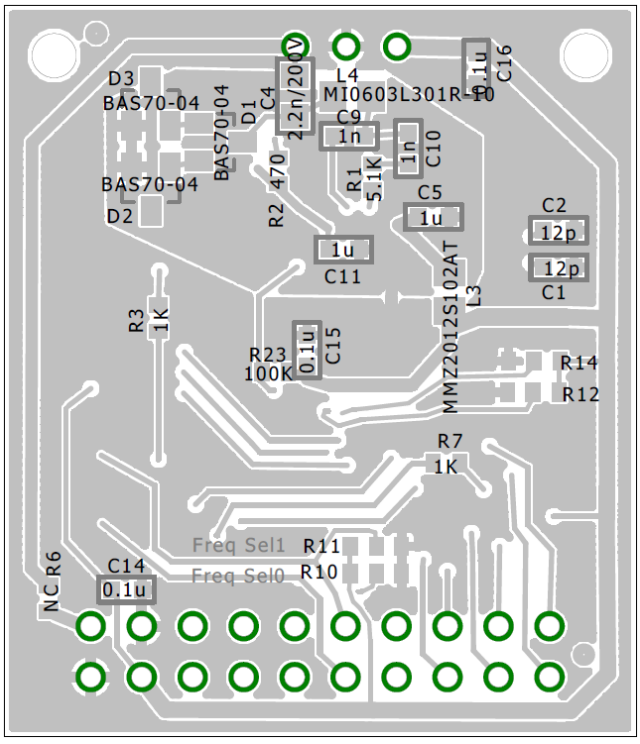
3. SIG102 PCB layout recommendation

Note: Analog ground layer and GND PLL should be connected to the digital ground near the Exp pad.

Top layer



Bottom layer



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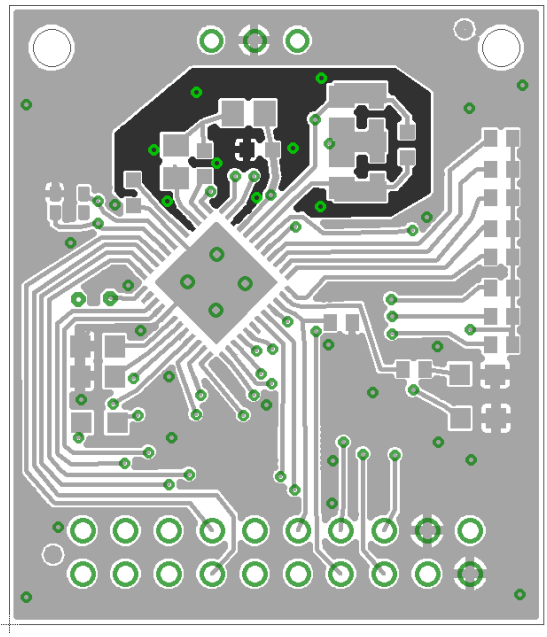
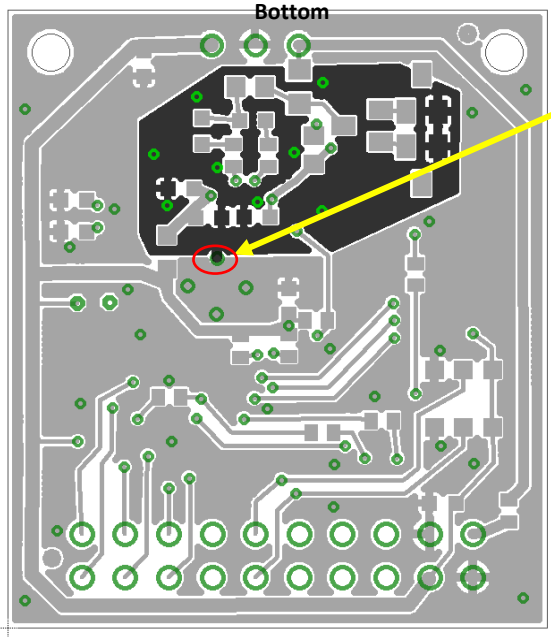
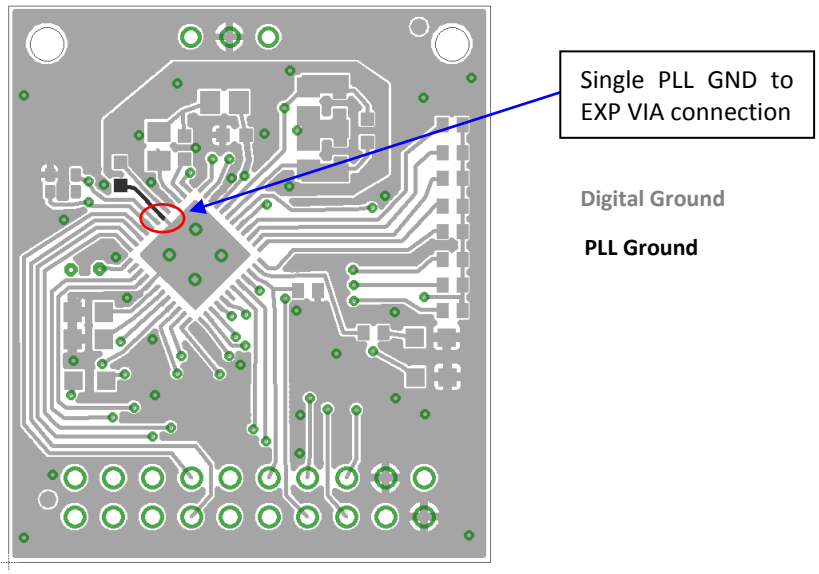
Top



Bottom



TOP - PLL Ground connection to EXP



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- ✓ VCC and DGND layout traces should be as wide as possible. Connect a 0.1uF capacitor between each VCC and DGND pins, as close as possible to the pins.
- ✓ It is recommended to keep the traces connecting the 3.3V power supply to VCC pins as short as possible with wide PCB traces.
- ✓ Connect AGND to EXP with a single short trace.
- ✓ Connect PLL_GND to EXP with a single short trace.
- ✓ Connect L1, L2, C13, C3, C5, C7, C8, C11, and C12 as close as possible to their pins.
- ✓ Connect R1 as close as possible to RXI pin.
- ✓ Connect all filtering caps as close as possible to their pins.
- ✓ Connect crystal and its capacitors close to OSCI and OSCO pins. Keep DGND plan around them.

4. SIG102 Package, Mechanical

The SIG102 is supplied in QFN 48 7mm x 7mm package.

4.1 Mechanical Drawing

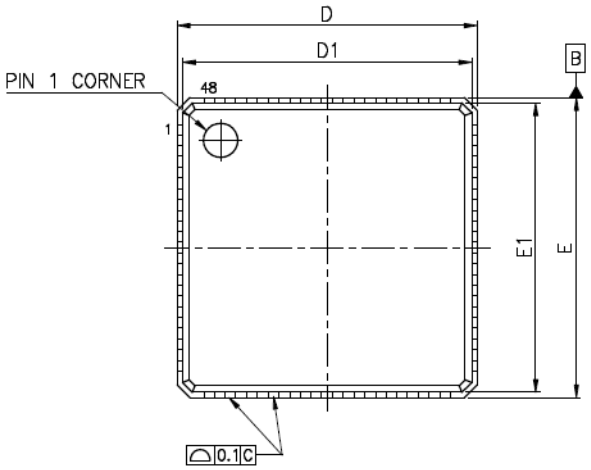
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.203 REF.	
b	0.18	0.25	0.30
c	0.24	0.42	0.60
D	6.90	7.00	7.10
D1	6.65	6.75	6.85
E	6.90	7.00	7.10
E1	6.65	6.75	6.85
e		0.50 BSC.	
K	0.20	—	—
L	0.30	0.40	0.50
θ°	0.00	—	12.00

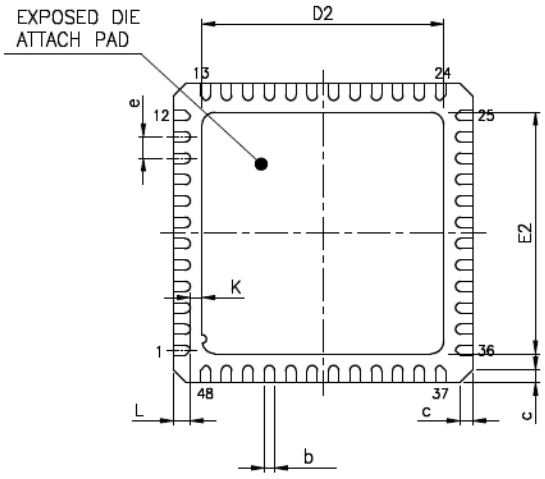
UNIT : mm

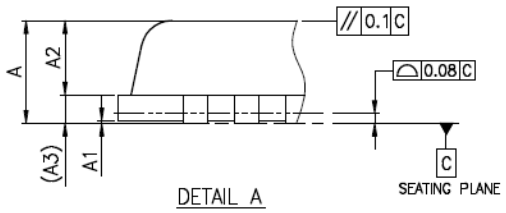
	D2			E2		
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
157X157MIL	3.40	3.60	3.80	3.40	3.60	3.80
213X213MIL	5.00	5.20	5.40	5.00	5.20	5.40
⚠ 208X208MIL	4.90	5.10	5.30	4.90	5.10	5.30

UNIT : mm

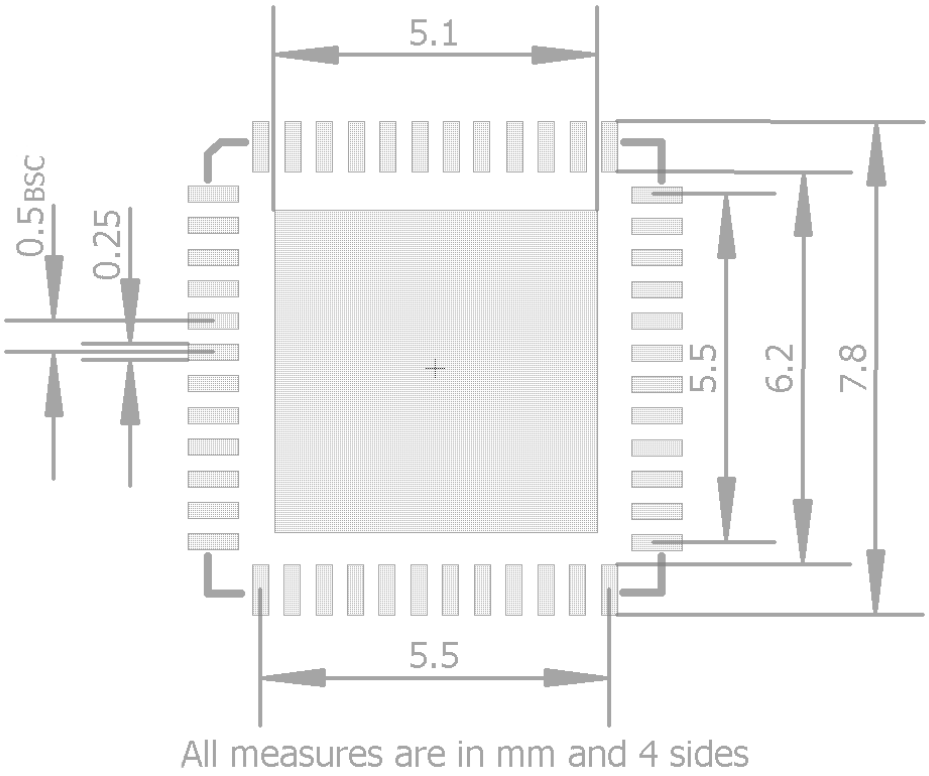
NOTES :
1. JEDEC : MO-220 VKKD-2.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION "b" APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. THE PIN #1 IDENTIFIER EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. DIMENSION "A1" APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.







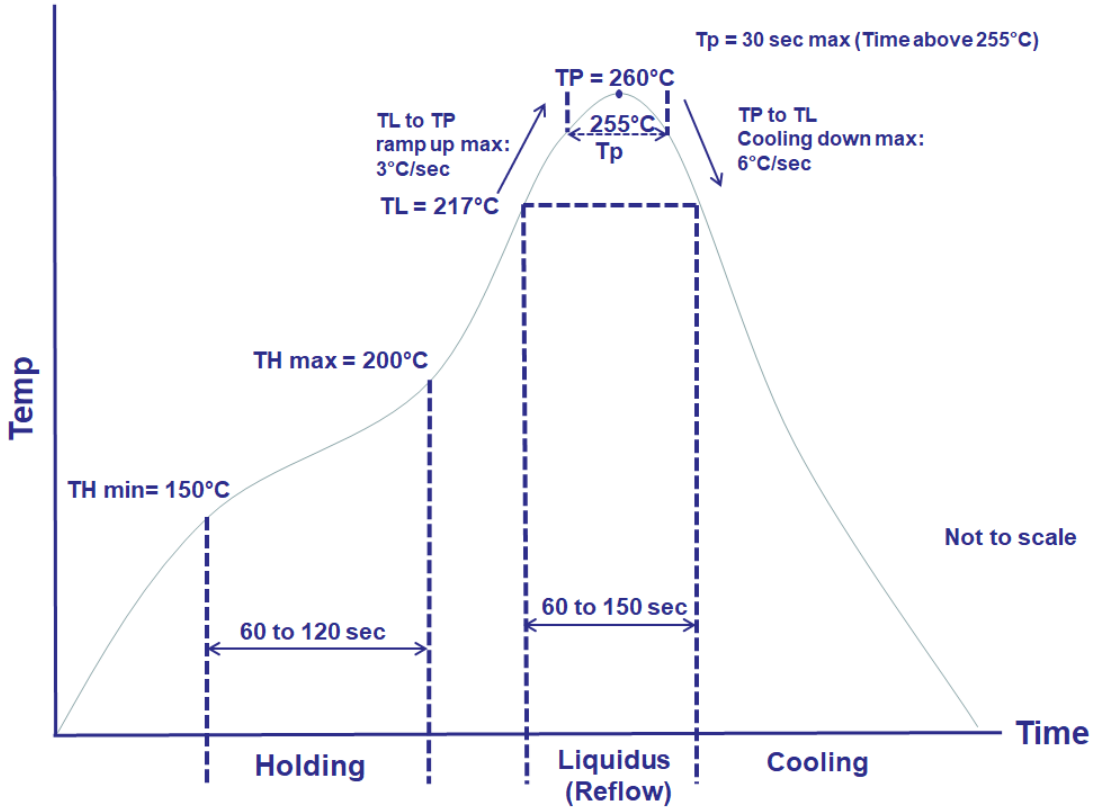
4.2 PCB Drawing



4.3 Soldering profile

Soldering reflow profile is according to IPC/JEDEC J-STD-020 (MSL3).

- Peak temperature (TP) is 260°C.
- Holding time is between 60 sec to 120 sec between TH min 150°C to TH max 200°C.
- Liquidus temperature (TL) is 217 °C. Liquidus time is between 60 sec to 150 sec.
- TL to TP max ramp up is 3°C/sec.
- TP to TL max cool down rate is 6°C/sec.
- Max time above 255°C (Tp) is 30 sec.



Representation of IPC/JEDEC J-STD-020 (MSL3) profile