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SIG61

Module Manual

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Revision History

Revision	Issue Date	Comments
0.1	23/12/2008	Preliminary beta addition
0.2	17/8/2009	Major updates
0.21	16/9/2009	4.2 checksum corrected
0.3	23/9/2009	JP2 pinout updated
0.4	12.10.2009	Interface with RS232 in SIG60 mode
0.41	28.12.2009	Updated protection network
0.5	16.8.2010	Updated to board Rev 3.1
0.501	18.8.2010	Updated J1 table, mechanical data updated
0.51	6.1.2014	Update the block schema (figure 2.1)
0.52	4.11.15	Update Table 3.1
0.53	24.4.17	Editing, 2.4
0.54	05.01.20	Update date

1. GENERAL

The SIG61 Independent Slave is a stand-alone solution for DC-BUS slave operating over the power lines, eliminating the need for a micro controller in the slave unit. Multiple SIG61 modules can communicate with at least one SIG60 operating as a master over the DC power line. An example of a system is presented in Figure 1.1.

The module contains all the required hardware for remotely reading its 8 input pins or writing to its 8 output pins by a SIG60 master. The hardware contains a line protection network, ceramic filters and a power supply. The Module performs an asynchronous UART protocol over DC power lines at predetermined bit rates. Each module can be configured to an ID address (0-15) by on board switches. The SIG61 respond to its master commands by either update its output pins or respond to a master command with a message containing its 8 input pins status. The SIG61 module can be interfaced directly to applications such as sensors or motors through its J1 I/O connector.

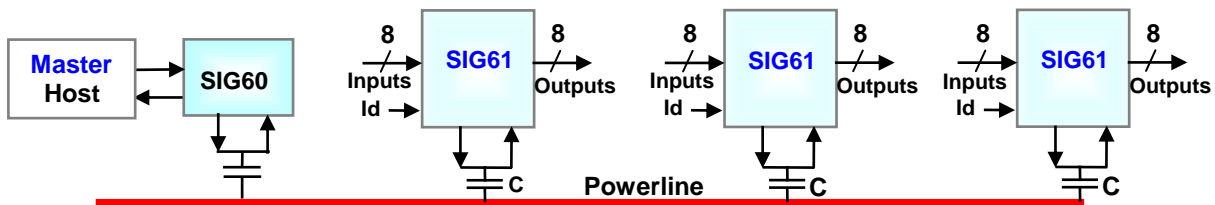


Figure 1.1 – SIG61s slave network example

2. Module Description

2.1. Block Diagram Description

The module is described in the block diagram of Figure 2.1

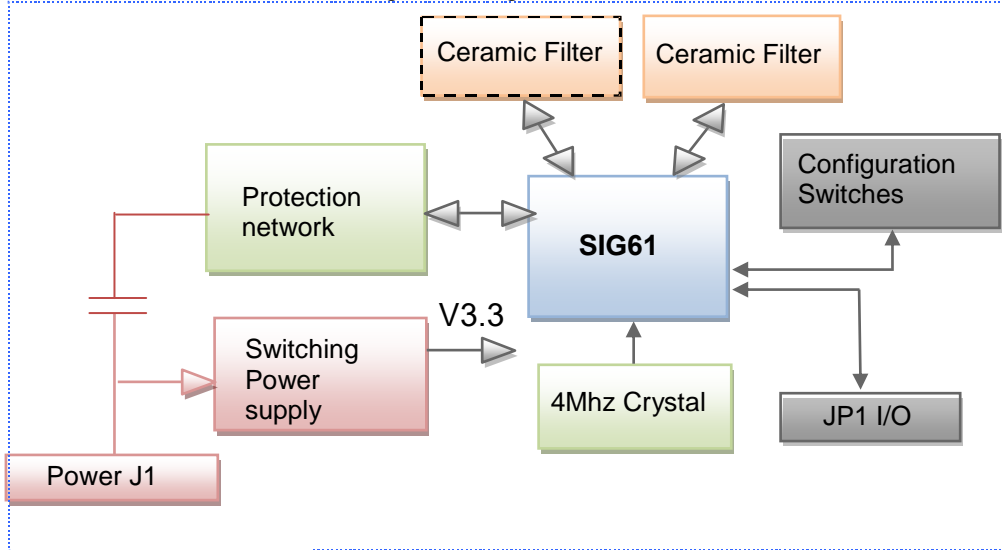


Figure 2.1 - SIG61 Board block diagram

The received data signal from the DC line passes a protection network, into RxIn input pin to a Rx amplifier. The amplified signal passes via F0B or F1B pins to an external ceramic filter and back into RxP input. Based on the decoded message, either data byte is transferred to the I/O connector output pins or the SIG61 respond with a message containing the status of the input pins on the I/O connector. The received message can be monitored on the HDO pin as an asynchronous bit stream.

The communication parameters (frequency, bit rate, etc.) are determined by the installed ceramic filter(s) and by the on-board switches.

The SIG61 respond to a master command by generating and transmitting a message from the DTXO pin. The digitally modulated signal passes to the ceramic filter for shaping. The shaped signal enters the SIG61 via F0B or F1B pins into an output amplifier. The modulated data on TxO pin drives the DC line via the protection network.

The on board switching power supply provides the 3.3V voltage required for the SIG61 operation. The power supply operates in a wide input voltage range between 10V and 36V. The module current consumption is in the range of 30mA depends on supply voltage.

2 .2. Hardware features:

- Noise robust DC Power Line Communication
- 8 remotely controlled Inputs
- 8 remotely controlled Outputs
- 16 selectable IDs
- Controlled by UART serial protocol
- Selectable data rates.
- Selectable operating frequencies.
- Use of low cost ceramic filter(s)
- Switching power supply for 10V to 36V operating voltage.
- Status indication LEDs.
- Small size board (60mmx40mm).
- 4MHz crystal.

Connectors:

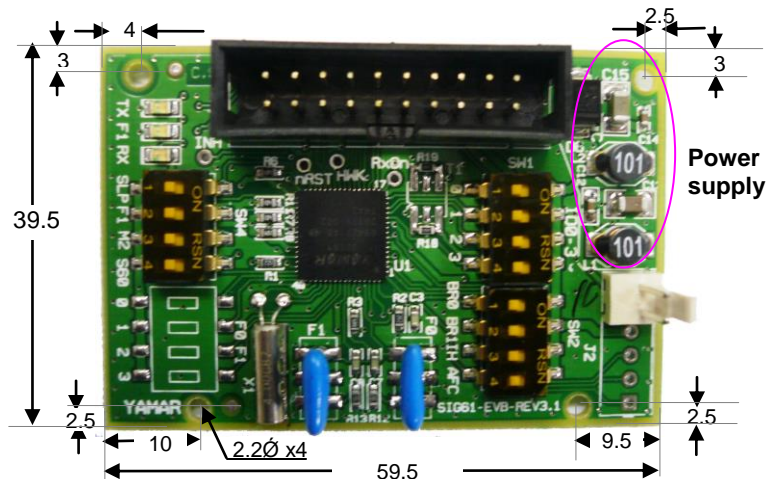
J1- I/O connector for activation of local commands and reading sensors.
J2 - Power input and Test points.

Display LEDs:

D4 - F1 indication LED. (On=F0)
D5 - Tx On LED indicates transmission.
D6 - Rx On LED, indicates a valid receive signal.

2 .3. Mechanical Data

Figure 2.2 show the module.



2.4. Configuration

The SIG61 mode of operation and its settings are configured according to its configuration switches (pins) as described in the SIG61 data sheet. When switches are in OFF position, the SIG61 operates in its default mode;

F0=5.5MHz, F1=6.5MHz, Bit rate = 19.2Kbps, ID=0, SIG60 mode.

Table 3.1 presents the SIG61 slave mode parameters.

When set to SIG60 mode, the device is configured by writing to its registers according to SIG60 data sheet.

Table 3.1 - Parameters and DIP-Switch setting

Switch	Parameter	Values
SW1 1-4	ID Address *	0 -15
SW2 1-2	Bit Rate	See data sheet
SW2 3	InterHop	On - Interference hope
SW2 4	Auto Frequency Change*	Off - Disable, On - Enable
SW3	Frequency set	Switch not installed
SW4 1	Auto Sleep	Off - Disable, On - Enable
SW4 2	F0_nF1	Off - F0, On - F1
SW4 3	Loop Back Disable	Off - Disable, On - Enable
SW4 4	SIG60/SIG61	Off - SIG60, On - SIG61

SWx On = "1" Off="0"

*In SIG61 mode only.

2.5. Module Connectors

2.5.1. J1 - I/O Interface Connector

Pin Name	Pin #	Pin Name	Pin #
SigO0	1	SigIn0	2
SigO1	3	SigIn1	4
SigO2	5	SigIn2	6
SigO3	7	SigIn3	8
SigO4	9	SigIn4	10
SigO5	11	SigIn5	12
SigO6	13	SigIn6	14
SigO7	15	SigIn7	16
Vcc (3.3V) output	17	Ground	18
*Vin –Power pin, when R19=0	19	HDO	20

All input signals are compatible with 3.3V CMOS logic.

2.5.2. J2 –DC Power Line and Test pins

Pins 5 and 6 are used for DC input. It is possible to use J1 connector for DC input by installing 0 ohm resistor in R19.

Power supply requirements: 10V to 36V, 30mA @12V.

Name	Pin #
TxO test-pin	1
TxOn test-pin	2
RxIn test-pin	3
3.3V output from power supply	4
GND	5
Power (& communication) input	6

All input signals are compatible with 3.3V CMOS logic

3. SIG61 Module Interfacing

3 .1. LIN over the DC line Interfacing

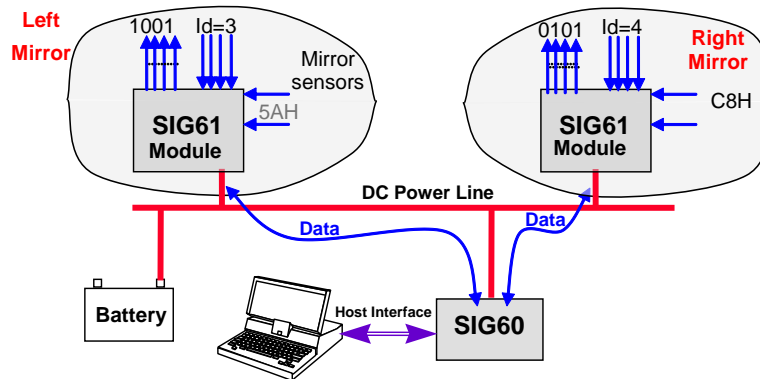


Figure 4.1 – SIG60 master and two SIG61 slave mirrors.

3 .2. Example - A master writes command to slave’s output pins

The master wishes to write 0110 to the Right mirror output pins. The master sends the following command:

0x00 (synch break), 0x55 (sync field), 0x14 (identifier), 0x06 (data byte), 0xE5 (check-sum).

3 .3. Example - A master reads command from slave’s input pins

The master wishes to read from the Left mirror. The master sends to the slave:

0x00 (synch break), 0x55 (sync field), 0x03 (Identifier)

The left mirror will respond with two bytes, the first is the status of its inputs and the second is the checksum of the Data byte and Identifier Byte.

4. Using SIG61 as a SIG60

Setting the switch SW4/S60 to OFF will change the SIG61 EVB to operate as SIG60 with few modifications. The configuration of the SIG60 can be made using the SIG60 internal registers.

Using this SIG60 mode of operation enables the Remote Loop Back feature causing the device to retransmit back to the bus its last received byte. When using this feature, the master device should allow time slot for the slave device to finish its retransmission before initiating a new transmission on the bus.

While operating in a SIG60 mode, connector J1 is used for HDI, HDO and HDC signals and Vcc and Ground. Figure 5.1 shows RS232 UART interface with SIG61 operating in SIG60 mode. For further information on the SIG60 operation, refer to SIG60 data sheet.

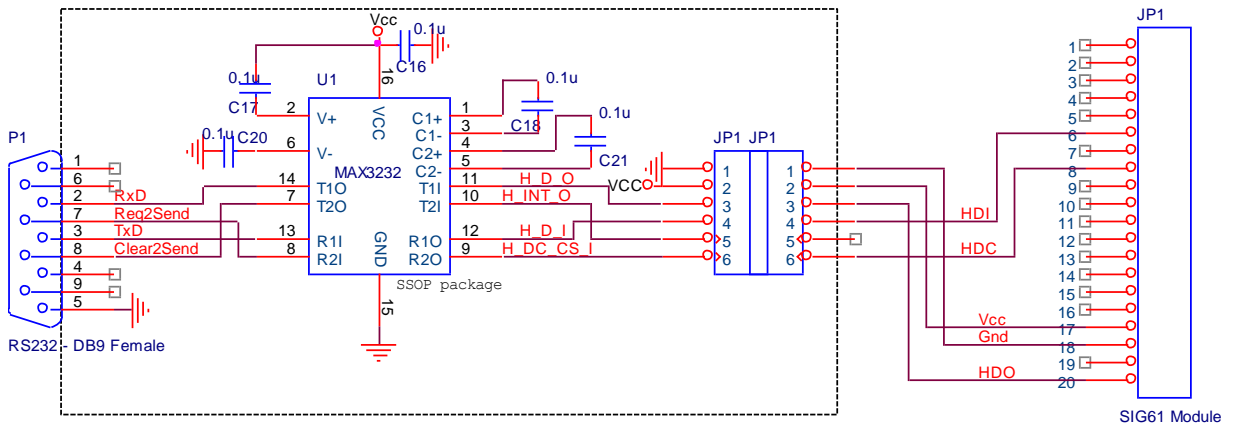


Figure 5.1 – SIG61 operating as SIG60 RS232 interface

5. Operation

1. Set the Module's configuration switches according to the required address, frequency, bit rate and operating mode.
2. Connect the module to the DC Power line.
3. Connect the desired output loads and input sensors to J2. Pay attention to the allowed output currents and input voltages.

Configure the Master SIG60 board to operate with same parameters as configured in the SIG61 board.

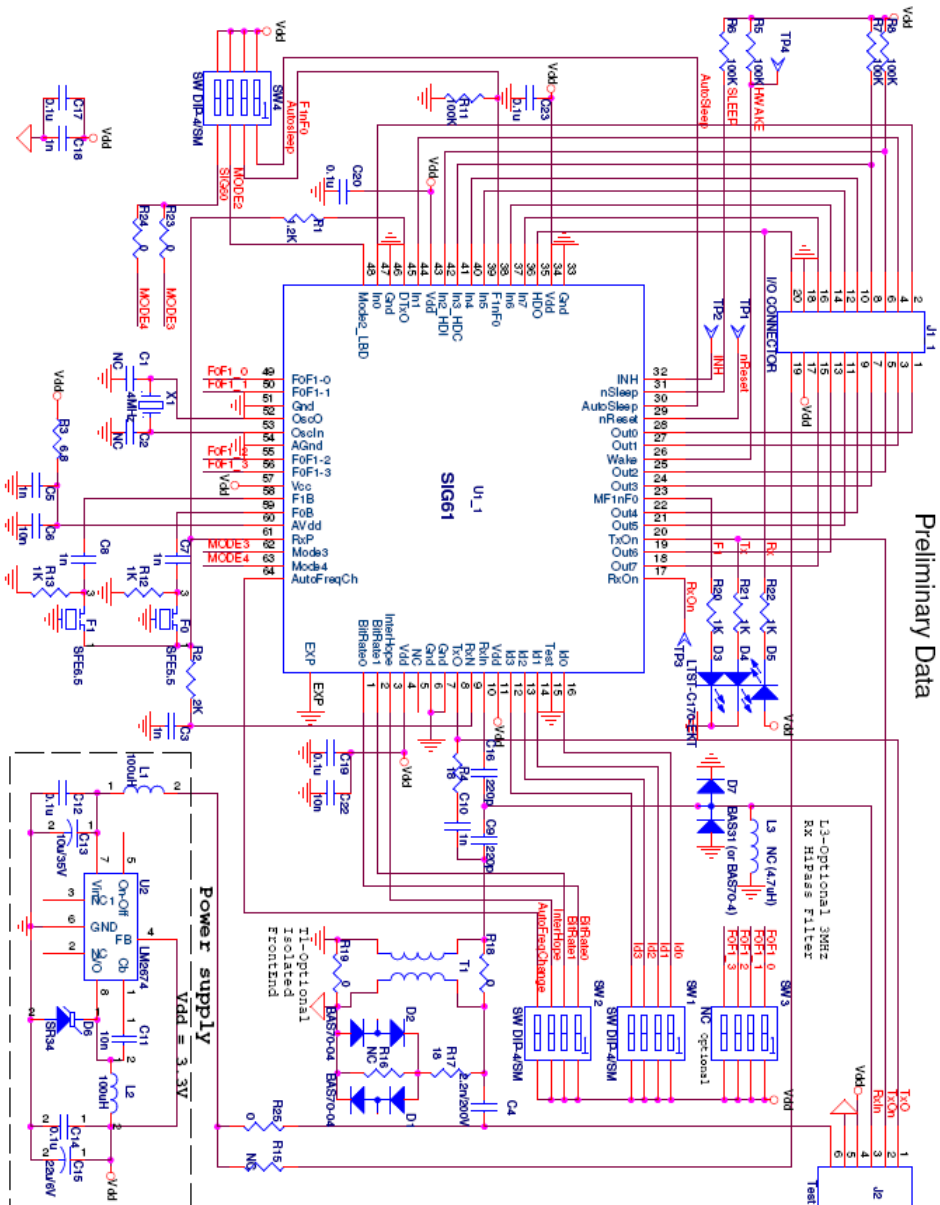


Figure 6 – SIG61 Schematics