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SIG60 EVB
Module Manual

Revision History

Revision	Issue Date	Comments
0.32	17.7.2011	Updated schematic L3=6.8uH
0.33	6.1.2014	Update block schema (figure 2.1)
0.331	17.1.2015	Upgraded board. Protection diode, LM2594 for operation up to 36V
0.34	28.11.17	Update connectors naming
0.35	05.01.20	Update date.

1. GENERAL

The SIG60 Module is designed to operate the SIG60 device in a system. Multiple SIG60 boards can communicate over a vehicle's DC power line using the UART interface. Network example is presented in Figure 1.1.

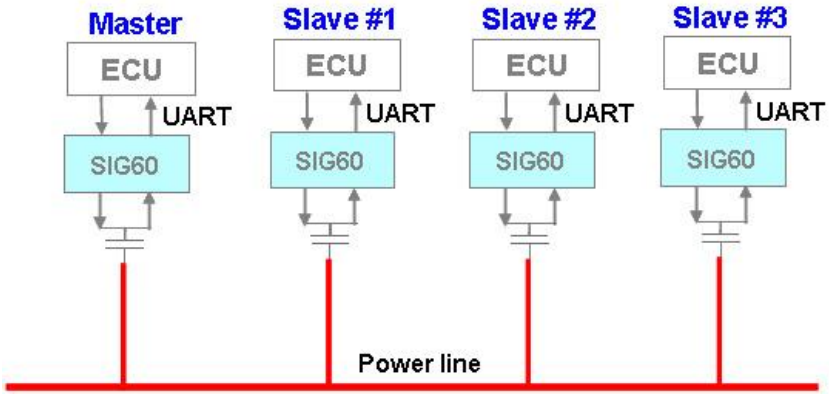

Figure 1.1 - System configuration example

2. SIG60 Board Description

2 .1. Block Diagram Description

The Module contains all the required hardware for device operation such as a line protection network, ceramic filters, and a power supply. The board performs an asynchronous UART protocol over DC power lines at data rates of up to 57.6Kbps. Operation at 115.2Kbps requires dedicated filters. The SIG60 may also be used as a new physical layer to the LIN protocol. The Module can be connected directly to a host (Micro controller with UART port or a PC) through its J1 I/O connector. The EVB block diagram is described in Figure 2.1.

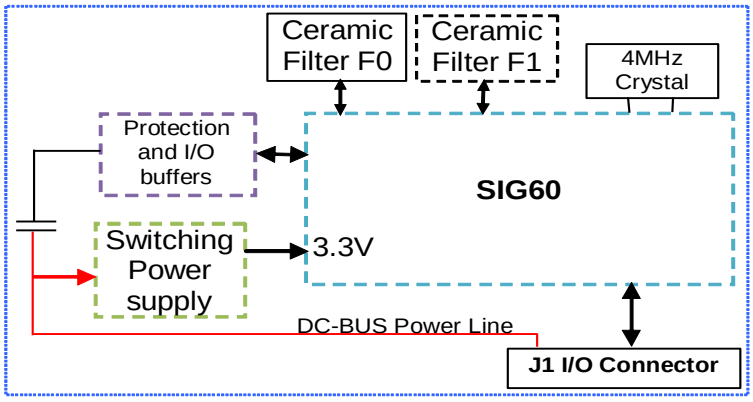

Figure 2.1 - SIG60 Board block diagram

The received data signal from the DC line passes through a protection network into the RxIn input pin to an Rx amplifier. The amplified signal passes via F0B or F1B pins to an external ceramic filter and back into Rxp input. The SIG60 decodes the data and output it to HDO pin as an asynchronous bit stream.

On the transmitter side, the host sends UART data to the SIG60 via HDI pin. The asynchronous data is protected against errors and modulated inside the SIG60. The DTXO pin outputs the digitally modulated signal to the ceramic filter for shaping. The shaped signal enters the SIG60 via F0B or F1B

pins into an output amplifier. The modulated data on TxO pin drives the DC line via the protection network. To connect HDI and HDO signals to a PC, additional RS232 or USB interface is required.

The switching power supply provides the 3.3V voltage required for the SIG60 operation. The power supply operates in a wide input voltage range between 10V and 36V. The module current consumption is in the range of 30mA depends on supply voltage.

The SIG60 internal registers, as described in the SIG60's datasheet, determine the operating communication frequency and bit rates. HDC signal is used for accessing the registers.

2 .2. Hardware features:

- Noise robust DC Power Line Communication
- UART serial interface
- Selectable data rates 9.6Kbps to 115.2Kbps
- One or two selectable operating frequencies
- Use of low cost ceramic filter(s)
- 10V to 36V operation using switching power supply
- Indication LEDs
- Small size board (40mm*27mm)

Connectors:

J1 - Host interface, configuration pins and Test I/O connector.
J2 - DC line connector and test points.

Display LEDs:

Tx LED - Indicates transmission.
Rx LED - Data output, indicates reception.
F1 LED - Indicates the selected channel (On=F1)

2 .3. Mechanical Data

The mechanical dimensions are shown in Figure 2.2.

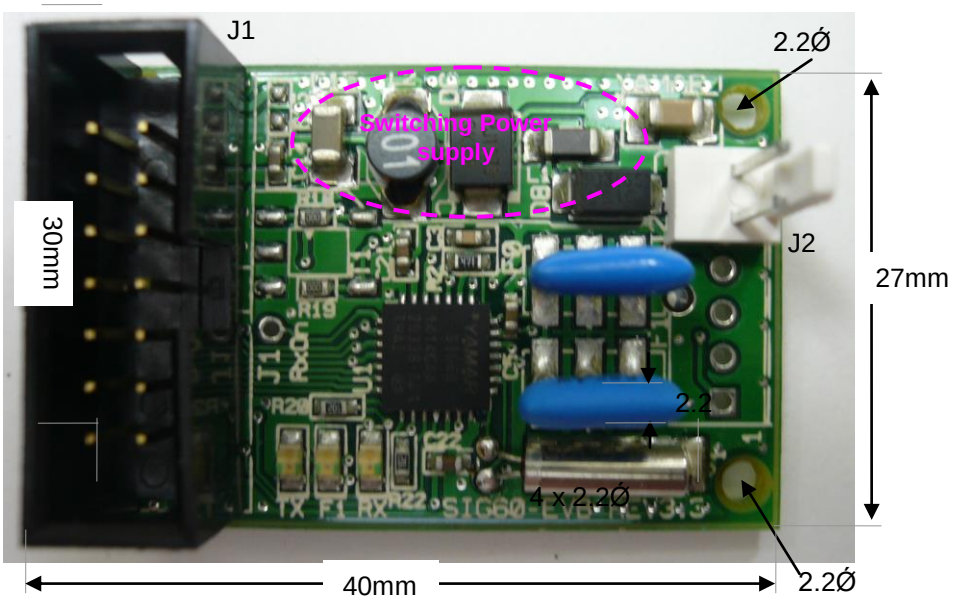

Figure 2.2 – SIG60 Module dimensions

3. Module Operation

3 .1. Configuration

The SIG60 mode of operation and its settings are configured at power-up, reset and whenever the Host writes into its internal register. Refer to SIG60 data sheet for further configuration information.

3 .2. Module Connectors

3.2.1. J1 – Host Interface Connector

Pin Name	Direction	Pin #	Pin Name	Direction	Pin #
HDO	O	1	INH	O	2
HDI	I	3	nSleep	I	4
HDC	I	5	nReset	I	6
Wake	I	7	InterfHop	I	8
F1nF0	I	9	MF0nF1	O	10
Vdd (3.3V) output	P	11	Ground	P	12
Ground	P	13	VBat (DC line) * Require R15 = 0 Ohm.	P	14

All input and output signals are compatible with 3.3V CMOS logic.

3.2.2. J2 – DC Power Line and test points

Name	Pin #
TxO test-pin	1
TxOn test-pin	2
RxI test-pin	3
3.3V output from power supply	4
GND	5
VBat DC line input	6

VBat input connects the module to the DC power line for communication and power supply.
Power supply requirements: 10V to 36V, 30mA. See Figure 3.1

3 .3. Interfacing to SIG60 Module

The SIG60 Module is designed to interface directly to any controller with UART port.
Three signals are essential for proper operation; HDI, HDO and GND (Data In, Data Out and Ground). All other signals are optional for reconfiguration (HDC), Sleep control, etc. Refer to SGI60 data sheet.
Figure 3.1 is an example for such an interface. It is recommended to add an inductor of at least 22uH between the SIG60 evaluation board and the Micro controller (uC) supply line to prevent influence of the uC power supply AC filter load on the SIG60 Module communication performance.
For operation other than the SIG60 default values, the HDC input has to be controlled by the host for more information.

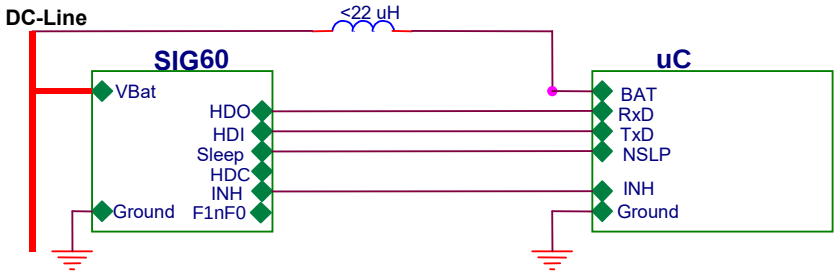

Figure 3.1 – SIG60 Module Interface with a Host.

3 .4. EVB Operation

1. The EVB operates at the default values of the SIG60 device. If the SIG60 device requires operation other than the default values, lower the HDC input and Write to the SIG60's registers the required bit rate and frequency settings as described in the SIG60's datasheet. Raise the HDC input and start UART communication. When using the default values (5.5MHz -6.5MHz, 19.2Kbps) there is no need for additional configuration.
2. Connect the communication signals via J1 to the host.
3. Connect the Modules to the DC Power line.
4. Transmit and receive data to and from remote host over the DC power line.
5. It is possible to change carrier frequency between F0 and F1 by using F1nF0 pin

3 .5. Evaluation board layout

Top view **Bottom view**

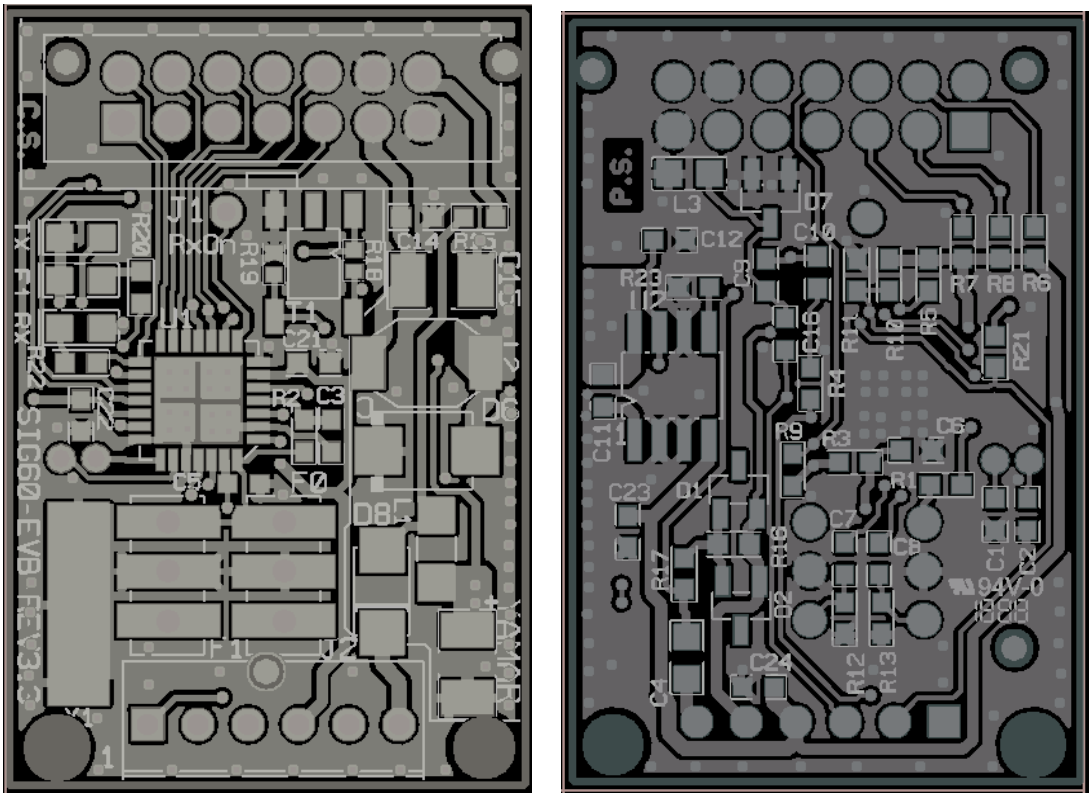

Figure 3.2 - SIG60 EVB Layout

3 .6. SIG60 EVB Schematic